PATENT APPLICATION
DOCKET NO.: 200207724-1

AMENDMENTS TO THE SPECIFICATION

Please replace Paragraph **[0002]** with the following amended paragraph:

[0002] This application discloses subject matter related to the subject matter disclosed in the following commonly owned co-pending patent applications: (i) "Programmable Clock Synchronizer," filed 7/30/2003; Application No. 10/630,159 (Docket No. 200207722-2), in the name(s) of: Richard W. Adkisson; (ii) "Controller Arrangement for a Programmable Clock Synchronizer," filed 7/30/2003; Application No. 10/630,182 (Docket No. 200207723-1), in the name(s) of: Richard W. Adkisson; (iii) "System and Method for Maintaining a Stable Synchronization State in a Programmable Clock Synchronizer," filed 7/30/2003; Application No. 10/630,297 (Docket No. 200208008-1), in the name(s) of: Richard W. Adkisson; (iv) "System and Method for Compensating for Skew between a First Clock Signal and a Second Clock Signal," filed 7/30/2003; Application No. 10/630,317 (Docket No. 200208009-1), in the name(s) of: Richard W. Adkisson; and (v) "Phase Detector for a Programmable Clock Synchronizer," filed 7/30/2003; Application No. 10/630,298 (Docket

No. 200208010-1), in the name(s) of: Richard W. Adkisson, all of which are incorporated by reference herein.

Please replace Paragraph **[0030]** with the following amended paragraph:

[0030] The following commonly owned co-pending U.S. patent applications describe the various functional blocks and sub-systems of the programable clock synchronizer system 100 in additional detail with respect to providing the overall functionality of controlling the bus clock and core clock synchronizers so as to properly synchronize data transfer operations even under variable skew and latency requirements: (i) "Programmable Clock Synchronizer," filed 7/30/2003; Application No. 10/630,159 (Docket No. 200207722-2), in the name(s) of: Richard W. Adkisson; (ii) "Controller Arrangement for a Programmable Clock Synchronizer," filed 7/30/2003; Application No. 10/630,182 (Docket No. 200207723-1), in the name(s) of: Richard W. Adkisson; (iii) "System and Method for Maintaining a Stable Synchronization State in a Programmable Clock Synchronizer," filed 7/30/2003; Application No.

10/630,297 (Docket No. 200208008-1), in the name(s) of: Richard W. Adkisson; (iv) "System and Method for Compensating for Skew between a First Clock Signal and a Second Clock Signal," filed 7/30/2003; Application No. 10/630,317 (Docket No. 200208009-1), in the name(s) of: Richard W. Adkisson; and (v) "Phase Detector for a Programmable Clock Synchronizer," filed 7/30/2003; Application No. 10/630,298 (Docket No. 200208010-1), in the name(s) of: Richard W. Adkisson, all of which are incorporated by reference herein.

Please replace Paragraph **[0040]** with the following amended paragraph:

[0040] A sync ratio sampling block 402 receives the M-bit wide sync_ratio_B 314 from the bus clock synchronizer controller portion 300 to generate a sync_ratio signal that is sampled in the core clock domain using the distributed core clock c 106'. FIG. 5B depicts an exemplary embodiment of the sync ratio sampling block 402 which synchronizes the sync_ratio_B signals from the bus clock domain by sampling them twice (for eliminating metastability) with two stages of flip flops clocked in the core clock domain to generate a sync_ratio signal 403. Since the clock frequency ratio

should not change once the ratio is detected in the bus clock domain (and sampled in the core clock domain), the system for coordinating the bus clock and core clock synchronizer controllers ensures that the value is stable by using a stable state detector block 412 of the core clock synchronizer controller portion. As described in the following cross-referenced U.S. patent application entitled "System and Method for Maintaining a Stable Synchronization State in a Programmable Clock Synchronizer," filed 7/30/2003; Application No. 10/630,297 (Docket No. 200208008-1), the stable state detector block 412 first waits for the clock ratio to be stabilized by determining that the sync_ratio signals do not change for a number of clock cycles in the core clock domain.